Remarks

This Amendment is responsive to the Office Action mailed June 29, 2006. Reexamination and reconsideration of claims 14-22, 33, 35, 37, and 48-76 is respectfully requested.

Summary of The Office Action

Claims 34 and 35 were objected to because both claims purportedly recited the same limitations. While claim 34 and 35 do recite the same limitations, they have different dependencies. Claim 34 has been cancelled.

Claims 33, 35, 37, 48, and 49 were objected to as being dependent upon a rejected base claim, but were identified as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These claims have been rewritten as suggested.

Claims 26-31 were rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. These claims have been cancelled.

Claims 1, and 3-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over O'Connor et al. (US Patent #6,532,531)(O'Connor) in view of Crouse et al. (US Patent #4,831,517)(Crouse). These claims have been cancelled.

Claims 2, 6-10, and 12-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over O'Connor and Crouse and further in view of Buckenmaier (US Patent #5,388,074)(Buck). These claims have been cancelled.

Claim 11 was rejected under 35 U.S.C. §103(a) as being unpatentable over O'Connor and Crouse and further in view of Dally et al(US Patent Publication #2003/0070059)(Dally). This claim has been cancelled.

Claims 14-17, and 23-25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Buck in view of Crouse. Arguments concerning claims 14-17 appear below. Claims 23-25 have been cancelled.

Claims 18-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Buck and Crouse and further in view of O'Connor. Arguments concerning these claims appear below.

Claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Buck, Crouse, and O'Connor and further in view of Dally. Arguments concerning this claim appear below.

Claims 26-31 were rejected under 35 U.S.C. §103(a) as being unpatentable over Buck in view of Dally. These claims have been cancelled.

Claim 32 was rejected under 35 U.S.C. §103(a) as being unpatentable over Daniel in view of Dally. This claim has been cancelled.

Claim 34 was rejected under 35 U.S.C. §103(a) as being unpatentable over Daniel and Dally and further in view of Crouse. This claim has been cancelled.

Claims 36, 38-39, 41-43, and 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Daniel in view of Dally and in view of Crouse. These claims have been cancelled.

Claims 40, 44-45, and 47 were rejected under 35 U.S.C. §103(a) as being unpatentable over Daniel, Dally and Crouse, and further in view of O'Connor. These claims have been cancelled.

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §103

To establish a prima facie case of 35 U.S.C. §103 obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143.01 Second, there must be a reasonable expectation of success. MPEP 2143.02 Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, none of the criteria described in MPEP 2143 are satisfied since there is no motive to combine the references, the combination of references is physically impossible, and even if combined (which is impossible) the combination of references does not teach or suggest all the claim limitations. None of the references, alone and/or in combination, teach receiving branch information, let alone branch information concerning branch resolution latency. Thus, none of the claims are obvious for at least this reason.

Buck

Buck describes a FIFO memory that uses a single output register to improve read-access time. (Abstract). The read-access time is improved by clocking the output register so that the FIFO output is provided with only the clock-to-output delay of the register. (Abstract). Buck describes that while "a need exists for improving the operating speed of a FIFO memory system in order to reduce overall access time ... **it is desirable that no major changes be made** to the circuit designs of the circuit elements of the memory system or to the supporting circuitry used with a conventional FIFO memory." C2, 140-45, emphasis added. Thus, Buck indicates that it should not be combined with other references that would

produce these major changes. Since Crouse describes adding a new instruction to a processor and since O'Connor describes stack processing, combining Buck with either of these references would require the major changes that Buck indicates should not be made. Thus, there is no motivation to combine the references, the combination of references would likely be inoperative, and even if combined the combination of references does not teach receiving branch information as claimed.

Crouse

Crouse describes a branch and return on address instruction for operating a digital data processor (Abstract). Crouse is "particularly useful for minimizing some of the problems associated with patching ROM code using RWM-loaded code." C1, l28-30. This appears to have nothing to do with improving read access time for a FIFO (Buck) proving that there is no motive to combine these references.

The benefit of Crouse is to provide "ROM patch capability in computer systems ... to avoid the considerable financial impact of updating systems in the field." C1, l32-35. Once again, this appears to be unrelated to improving FIFO performance (Buck), and thus yielding no motive to combine.

The Office Action asserts that Crouse teaches receiving information that a pop request was speculative. The OA provides no pinpoint citation to a passage that teaches this element. The Office Action explains that "returning to the instruction following the patch hook (restoring a state of the pop pointer) if there is no corrective code means that the pop request was speculative." Page 11. However, none of the cited passages, or indeed any portion of Crouse describe "receiving information to indicate at least one of the one or more pop requests was speculative." Furthermore, Crouse describes that the branch from the ROM to the RWM is "unconditional". Something that is unconditional simply cannot be speculative.

Concerning the combination of Buck and Crouse, Crouse provides an instruction that can be inserted into a RWM (read write memory) to alter how a ROM code operates. Buck concerns a FIFO memory that does not store instructions. The instruction for changing how a ROM can be updated could not be added to Buck. Similarly, the clocking added to the

output register of Buck could not be added to Crouse. Thus, the proposed combination is physically impossible to implement.

The combination of references does not teach receiving branch information. Additionally, there is no motive to combine, particularly in light of the teaching in Buck that no modifications to circuits interacting with the FIFO should be made. No motivation can be found to combine Buck (improve read access time for a FIFO) with Crouse, which describes itself as having "a primary purpose ... to provide a new processor instruction for enabling patch code segments to be provided which do not require the duplication in RWM of any good and valid ROM instructions." C6, l16-20.

Claims will now be discussed individually.

Claims 14-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Buck in view of Crouse.

Independent Claim 14

This claim is directed to a method for a FIFO memory. This claim recites, among other things, receiving information to indicate that a pop request was speculative. The combination of references does not disclose receiving this type of information.

The Office Action reports that Buck purportedly teaches processing a pop request but admits that Buck does not teach storing prior pop pointer values, receiving information that a pop was speculative and that a pop pointer should be restored, and restoring the pop pointer. So, Crouse must contain the missing receiving of information.

The Office Action asserts that Crouse teaches receiving information to indicate at least one of the pop requests was speculative. The Office Action relies on C2, l21-44 and C5, l4-46 to support the assertion. However, C2, l21-44 simply describes how a branch instruction works, without describing the receipt of any branch information, let alone information that a branch was speculative. Similarly, C5, l4-46 simply describes how conventional patch hook processing includes unconditional branches, without describing the receipt of any branch information. While a pop pointer value may be stored and restored, the

storing and/or restoring is unrelated to the receipt of any information, let alone the receipt of information indicating that a pop request was speculative.

Since this claim recites features not taught or suggested by the reference, it patentably distinguishes over the reference. Accordingly, dependent claims 15-22 also patentably distinguish over the reference and are in condition for allowance.

Dependent Claims 15-22

These claims were rejected under 35 U.S.C. §103(a) as being unpatentable at least over Buck in view of Crouse. As these claims depend from claim 14, the arguments above apply equally to these claims. Accordingly, these dependent claims distinguish at least over Buck in view of Crouse and are in condition for allowance.

Claims 18-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Buck and Crouse and further in view of O'Connor.

Buck and Crouse have been described above.

O'Connor

O'Connor describes a memory architecture that improves the speed of method invocation by storing method frames of method calls in two different memory circuits. (Abstract). O'Connor uses **stacks** for the memory circuits. (Abstract) While stacks use push and pop operations, stacks are not FIFO (first-in first-out) memories. Rather they are FILO (first-in last-out) memories. Thus, any proposed combination of Buck and O'Connor is impossible and therefore there is no motive to combine these references. If the references were combined, the result would be inoperative, yielding no expectation of success. Furthermore, the combination of references still would not teach receiving information to indicate that a pop request was speculative. For at least these reasons claims 18-21 are not obvious and are in condition for allowance.

Claim 18

This claim depends from claim 17, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally, this claim describes determining a status of the memory array in response to the pop pointer value and the push pointer value. The Office Action asserts that O'Connor teaches reading a pop pointer value ... and determining a status of the memory array. The Office Action relies on C3, l19-65, C4 L1-8, C30 l31-58 and Fig. 10A to support this assertion.

C3, l19-65 describes stack management and determining whether a stack is full.

C4 L1-8 also describes stack management and determining whether a stack is full.

C30 l31-58 describes high-water mark and low-water mark heuristic programming for a dribble manager unit 151, which interacts with a stack.

Fig. 10A illustrates the dribble manager unit 151.

All of these passages, and indeed all of O'Connor describe stack operations, which simply cannot be added to the FIFO processing of Buck. While a push and pop pointer may be read, they are push and pop pointers for a stack and thus are not push and pop pointers as claimed. Even if combined, no information that indicates that a pop request was speculative is received.

Thus, there is no motive to combine the references, it is physically impossible to combine the references yielding no expectation of success, and even if combined the references still do not teach every element of the claim. For at least this reason claim 18 is not obvious and is in condition for allowance.

Claim 20

This claim depends from claim 19, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally, this claim describes how a high threshold level is responsive, at least in part, to a maximum branch resolution latency. The Office Action asserts that O'Connor teaches responsiveness to the maximum branch latency. The Office Action relies on C3, l19-65, C4, l1-8, C19, l9-16, C19, l46-62, and C30, l31-58 to support the assertion.

C3, l19-65 describes stack management and determining whether a stack is full.

C4, l1-8 also describes stack management and determining whether a stack is full.

C19, l9-16 describes handling a stack overflow or underflow condition by generating a pipeline stall signal.

C19, l46-62 describes stack management unrelated to branch resolution latency.

C30, l31-58 describes dribble manager processing based on read and write rates.

Thus, none of these passages teach making a high threshold responsive to a maximum branch latency. The Office Action asserts that underflow and overflow are branch resolution latency. This is simply incorrect. Underflow and overflow as described in O'Connor are related to read and write rates to a stack, and are unrelated to branch resolution latency. For this additional reason this claim is not obvious and is in condition for allowance.

Claim 21

This claim depends from claim 20, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally, this claim characterizes maximum branch latency. The Office Action asserts that maximum branch resolution latency is the depth of an instruction pipeline in a processor, where the processor couples to the FIFO memory. The Office Action relies on O'Connor, however O'Connor concerns stack processing, not FIFO processing. The Office Action specifically relies on C11, l59-67, C12, l19-22, C15, l34-40, and C19, l9-16.

C11, l59-67 describes nothing relating branch resolution latency to instruction pipeline length.

C12, l19-22 reads "[t]he front end of hardware processor 100 is largely separate from the rest of hardware processor 100. Ideally, one instruction per cycle is delivered to the execution pipeline." Thus, this passage clearly teaches nothing relating branch resolution latency to instruction pipeline depth.

C15, l34-40 mentions a short pipe with a quick branch resolution. While the words "branch" and "resolution" appear in this passage, nothing tying instruction pipeline depth to branch resolution latency is described.

C19, l9-16 describes handling a stack overflow or underflow by generating a pipeline stall signal. There is no FIFO, and thus no processor connected to a FIFO. Also, there is no tying of the depth of a pipeline processor to branch resolution latency.

Thus, the combination of references does not teach that a high threshold level is responsive to the lesser of a maximum branch resolution latency and the low threshold level as claimed. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 22

Claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Buck, Crouse, and O'Connor and further in view of Dally. Cobbling together four references appears to be impermissible hindsight reconstruction. Even though four references have been combined, the combination of references still does not teach all the claimed elements.

This claim depends from claim 20, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally, this claim describes that received information includes maximum branch latency and then characterizes maximum branch latency. This claim characterizes branch resolution latency as the number of instruction cycles to resolve a branch instruction in a processor. The Office Action asserts that Dally p1, P11 teaches that branch information includes branch resolution latency characterized as claimed. The passage defines branch latency. However, it fails to teach that this information is received in branch information available to the claimed method. Since the information is not received, the combination of references still fails to teach all the claimed elements. For this additional reason this claim is not obvious and is in condition for allowance.

Ascertaining Skill Level of One Skilled In The Art

The MPEP requires that the Office Action ascertain and describe the level of ordinary skill so that objectivity can be maintained. MPEP §2141.03 reads:

> The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry. *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718, 21 USPQ2d 1053, 1057 (Fed. Cir. 1991). The examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time the invention was made, and not to the inventor, a judge, a layman, those skilled in remote arts, or to geniuses in the art at hand. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 218 USPQ 865 (Fed. Cir. 1983), *cert. denied*, 464 U.S. 1043 (1984).

Here the Office Action neither ascertains nor reports on the level of ordinary skill in the art. For this additional reason all the obviousness rejections are improper.

Conclusion

For the reasons set forth above, **claims** 14-22, 33, 35, 37, and 48-76 patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

JOSE S. NIELL ET AL.
By their Representatives,
Customer Number 62442

JOHN T. Kalnay (Reg. No. 46,816)
(216) 348-5844

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Laura Bray
Name

Laura Bray
Signature